METHOD OF FORMING FINE PATTERNS

Background of the Invention

Field of the Invention

The present invention relates to a method of forming fine patterns of a thin film on a substrate in the process of manufacturing a semiconductor device and the like.

Background Art

Figs. 1A, 1B, 1C, and 1D are diagrams showing a conventional method of forming patterns that uses a lithography technique.

As Fig. 1A shows, an oxide film 2 of a thickness of about 4 nm is formed on a semiconductor substrate 1 such as a silicon wafer. A polysilicon film 3 of a thickness of about 150 nm is formed on the oxide film 2, and an oxide film 4 of a thickness of about 200 nm is formed on the polysilicon film 3. Next, an organic anti-reflective film 6 of a thickness of about 100 nm is formed on the oxide film 4, and a resist pattern 7 of a line-and-space (hereafter referred to as L/S) of 0.16/0.16 μm is formed on the anti-reflective film 6 with lithography equipment such as an excimer laser.

Next, as Fig. 1B shows, the anti-reflective film 6 is etched with the resist pattern 7 as a mask. Etching is performed using dry etching equipment so as not to change the line width of the resist pattern 7.

Furthermore, as Fig. 1C shows, the oxide film 4 is etched using oxide-film etching equipment.

Thereafter, as Fig. 1D shows, the resist pattern 7 is removed by ashing. Then, the polysilicon film 3 is etched with silicon dry etching equipment using the oxide film 4 as a hard mask.

As obviously seen in Fig. 1D, the pattern of the polysilicon film 3 formed by the above-described process is of the L/S = 0.16/0.16 μm, identical to the L/S of the resist pattern 7.

In this method, since a thin film pattern is fabricated using a resist pattern formed with a lithography technique (hereafter referred to as "lithography pattern") as a mask, a pattern finer than the lithography pattern cannot be formed.

Although a slimming technique has been known as a method of narrowing the line width, since the space width is widened as the line is narrowed, the pattern pitch does not change from the resist pattern, and the pattern does not become finer.

Summary of the Invention

The object of the present invention is to provide a method of forming a fine pattern without being obstructed by the limitation of a lithography technique.

First, a resist pattern is formed using a lithography technique on a film to be processed that has been deposited on a substrate. The resist pattern is subjected to etching to narrow the line width. Next, the first film to be processed underneath the resist pattern is subjected to anisotropic etching under a reduced pressure. Etching under a reduced pressure accelerates the etching rate in the vicinity of the side of the line of the pattern compared to other areas. Therefore, when difference in the etching rates is utilized, the underlying film to be processed can be exposed in the vicinity of the side of the line of the pattern, leaving the film to be processed in other areas. This etching exposes only the vicinity of the side of the line of the resist pattern of the second film to be processed underneath the first film to be processed, and forms the pattern of the first film to be processed. Next, the second film to be processed is etched using the pattern of the first film to be processed as a mask to form the pattern of the second film to be processed. The pitch of the resulting pattern of the second film to be processed becomes 1/2 the pitch of the resist pattern.

Other and further objects, features and advantages of the invention will appear more fully from the following description.

Brief Description of the Drawings

The present invention will be more apparent from the following detailed description, when taken in conjunction with the accompanying drawings, in which;

Figs. 1A, 1B, 1C, and 1D are diagrams showing a conventional method of forming patterns;

Figs. 2A, 2B, 2C, 2D, 2E, 2F, and 2G are diagrams showing a method of forming a fine pattern according to the present invention.

Detailed Description of the Preferred Embodiments

First, as Fig. 2A shows, films to be processed are deposited on a semiconductor substrate 1 such as a silicon wafer. To begin with, an oxide film 2 of a thickness of about 4 nm is formed, and a polysilicon film 3 of a thickness of about 150 nm is formed on the oxide film 2. An oxide film 4 of a thickness of about 100 nm is formed on the polysilicon film 3, and a nitride film 5 of a thickness of about 30 nm is further formed on the oxide film 4. An organic anti-reflective film 6 of a thickness of about 100 nm is applied to the nitride film 5.

Here, the nitride film 5 corresponds to the above-described first film to be processed, and the oxide film 4 corresponds to the above-described second film to be processed. The polysilicon film 3 is the third film to be processed.

Next, a resist pattern 7 of an L/S of 0.16/0.16 μm is formed on the anti-reflective film 6 with lithography equipment such as an excimer laser (lithography step).

Then, as a first etching step, the resist pattern 7 is subjected to slimming. In this embodiment, dry etching equipment and resist ashing equipment are used, and a gas that contains O_2 is used. In this case, as Fig. 2B shows, conditions are set so that the resist pattern 7 also etched in the lateral direction, and that L/S becomes 0.12/0.20 μm. In this step, the resist

pattern 7 is slimmed, and at the same time, and the anti-reflective film 6 is etched using the resist pattern 7 as a mask. In the following description, the anti-reflective film 6 is treated as a part of the resist pattern 7.

Next the second etching step will be described. The second etching step is performed using silicon dry etching equipment of for example an ECR type, under the following conditions.

[Etching Conditions]

Pressure: 1 Pa, microwave power: 800 W, bias power: 200 W, process gas: Cl_2: 200 sccm

In dry etching under such a low pressure, the etching rate in the vicinity of the side of the pattern is higher than the etching rate in other portions. As a result, the underlying oxide film 4 is exposed only in the vicinity of the side of the pattern, and a new mask pattern of the nitride film 5 can be formed in the area that was a space in the resist pattern 7.

It is preferable that etching is conducted so as to equalize the widths of the area where the nitride film 5 remains, that is, the area to be the mask in the third etching step described below, with the widths of the resist pattern 7, regardless of the presence or absence of the upper-layer resist. In the embodiment, since the L/S of the resist pattern 7 is made 0.12/0.20 μm by the first etching step (Fig. 2B), if the width of the opened area of the nitride film 5, that is, the area to expose the oxide film 4 by etching is 0.04 μm, the line width of the pattern of the newly formed nitride film 5 becomes 0.12 μm, which equals to the line width of the resist pattern.

As a third etching step after removing the resist pattern 7 (including the anti-reflective film 6) by ashing, the oxide film 4 is subjected to dry etching and wet etching using the nitride film 5 as a mask to form the pattern of the oxide film 4.

Fig. 2D is a diagram showing the pattern of the oxide film 4 formed by dry etching. At this time the pattern with a pitch of a half the pitch of the resist pattern 7 can be obtained. Also,

the L/S of the pattern obtained by the third etching step becomes 0.12/0.04 μm, while the L/S of the resist pattern 7 was 0.16/0.16 μm.

Next, wet etching is conducted so that the L/S becomes a desired L/S within a range between 0.12/0.04 μm and 0.04/0.12 μm. However, dry etching may also be used if it is isotropic.

In the case of oxide-film etching, since the nitride film 5 on the upper surface of the oxide film 4 is not etched, and the width of the nitride film 5 is unchanged, the nitride film 5 is then removed by nitride-film etching (Fig. 2F).

In a fourth etching step, the polysilicon film 3 is etched using the pattern of the oxide film 4. Fig. 2G shows the structure finally obtained when etching is conducted so that the L/S of the pattern of the oxide film 4 becomes 0.08/0.08 μm in the above-described third etching step. In this case, the obtained pattern has the pitch, line width and space of a half the pitch, line width and space of the resist pattern 7.

By forming gate electrodes from the pattern formed as described above and forming a source/drain region on the semiconductor substrate 1 by the ordinary process, a semiconductor device of a higher density than conventional semiconductor devices can be manufactured.

To summarize, the method of this embodiment is a method of forming a fine pattern that has a pitch half the pitch of a lithography pattern, by narrowing the line width of the resist pattern by slimming in the first etching step; forming a new mask pattern in the space widened by slimming in the second etching step; and etching the underlying layer using the mask pattern in the third etching step.

The reason why wet etching is conducted as well as dry etching in the third etching step is that since etching is conducted in the second etching step utilizing difference in etching rate in a reduced-pressure environment, it is difficult to form the pattern of the desired size. For example, if the etching time

is increased to reduce the line width, the portion to be left as a line is etched, and the required thickness cannot be secured. Therefore, a desired line width is obtained by isotropic etching in the third etching step. However, even if isotropic etching is not conducted, the pattern pitch can be made half the pitch of the lithography pattern; therefore, isotropic etching is not essential in the present invention.

Although desired line widths and space widths can be obtained when isotropic etching in the third etching step is conducted, the shape of the obtained pattern is not always suitable to form the components of the semiconductor device (e.g., the gate electrode). In this embodiment, therefore, anisotropic etching is further conducted also using the pattern obtained by the isotropic etching as a mask (the fourth etching step) to obtain the pattern of the desired shape that has the pitch of half the pitch of the lithography pattern, and desired line widths and space widths. However, the fourth etching step is only preferable to adjust the shape of the pattern, and is not essential in the present invention.

Although the materials for the film to be processed is not specifically limited in the method of the present invention, since the underlying film to be processed is etched using the pattern of upper-layer film to be processed as a mask in each etching step, the combination of film materials having corresponding etching selectivity. For example, in the third etching step, since the second film to be processed is etched using the pattern of the first film to be processed as the mask, it is required, also considering the combination with the etching gas, to select a combination in which the etching rate of the second film to be processed is higher than the etching rate of the first film to be processed, and preferably, the rate ratio is as large as possible.

Although a silicon substrate is used as the semiconductor substrate 1, silicon oxide films are used as the oxide film 2

and the oxide film 4, and a silicon nitride film is used as the nitride film 5, the materials for the substrate and films may be other materials as far as the above-described requirements for etching rates are satisfied. Since the oxide film 4 and the nitride film 5 are not necessarily required to be the oxide film and the nitride film of the semiconductor substrate, the oxide film 4 and the nitride film 5 are not limited to a silicon oxide film and a silicon nitride film, respectively, even if the semiconductor substrate is a silicon substrate.

In this embodiment, although the finally formed pattern is the pattern of the polysilicon film 3, the conductive film is not limited to a polysilicon film, but tungsten film, tungsten silicide film, or the like may be used.

The method of the present invention can be applied not only to the case where a gate electrode and the like disposed on a substrate is formed, but also to the case where a wiring pattern disposed in an interlayer insulating film is formed. The method of the present invention is not limited to the formation of a conductive film pattern, but is applicable to the formation of an insulating film pattern.

It is further understood that the foregoing description is a preferred embodiment of the disclosed apparatus and that various changes and modifications may be made in the invention without departing from the spirit and scope thereof.

The entire disclosure of a Japanese Patent Application No.2001-007539, filed on January 16,2001 including specification, claims drawings and summary, on which the Convention priority of the present application is based, are incorporated herein by reference in its entirety.